IN THE SPECIFICATION:

Please amend the first full paragraph on page 2 as follows:

Field of the Invention: The present invention relates to an apparatus and a method for increasing semiconductor device density. In particular, the present invention relates to a vertical multi-chip device using combined ~~flip chip~~ flip-chip and wire bond assembly techniques to achieve densely packaged semiconductor devices, and a method for producing such devices.

Please amend the fourth full paragraph on page 2 as follows:

COB - Chip On Board: The techniques used to attach semiconductor dice to a printed circuit board, including ~~flip chip~~ flip-chip attachment, ~~wirebonding,~~ wire bonding, and tape automated bonding ("TAB").

Please amend the sixth full paragraph on page 2 as follows:

~~Flip Chip~~ Flip-Chip Attachment: A method of attaching a semiconductor die to a substrate in which the die is inverted so that the connecting conductor pads on the face of the device are set on mirror-image pads on the substrate (such as a printed circuit board), and bonded by solder reflux or a conductive polymer curing.

Please amend the second full paragraph on page 3 as follows:

State-of-the-art COB technology generally consists of three semiconductor die to printed circuit board conductive attachment techniques: ~~flip chip~~ flip-chip attachment, ~~wirebonding,~~ wire bonding, and TAB.

Please amend the third full paragraph on page 3 as follows:

~~Flip chip~~ Flip-chip attachment consists of attaching a semiconductor die, generally having a BGA, an SLICC or a PGA, to a printed circuit board. With the BGA or SLICC, the solder or other conductive ball arrangement on the semiconductor die must be a mirror-image of the connecting bond pads on the printed circuit board such that precise connection is made. The

semiconductor die is bonded to the printed circuit board by refluxing the solder balls. With the PGA, the pin arrangement of the semiconductor die must be a mirror-image of the pin recesses on the printed circuit board. After insertion, the semiconductor die is generally bonded by soldering the pins into place. An under-fill encapsulant is generally disposed between the semiconductor die and the printed circuit board for environmental protection and to enhance the attachment of the die to the board. A variation of the pin-in-recess PGA is a J-lead PGA, wherein the loops of the ~~J's~~ Js are soldered to pads on the surface of the circuit board. Nonetheless, the lead and pad locations must coincide, as with the other referenced flip-chip techniques.

Please amend the paragraph bridging pages 3 and 4 as follows:

~~Wirebonding~~ Wire bonding and TAB attachment generally begins with attaching a semiconductor die to the surface of a printed circuit board with an appropriate adhesive, such as an epoxy. In ~~wirebonding,~~ wire bonding, a plurality of bond wires ~~are~~ is attached, one at a time, to each bond pad on the semiconductor die and extend to a corresponding lead or trace end on the printed circuit board. The bond wires are generally attached through one of three industry-standard ~~wirebonding~~ wire bonding techniques: ultrasonic bonding - using a combination of pressure and ultrasonic vibration bursts to form a metallurgical cold weld; thermocompression bonding - using a combination of pressure and elevated temperature to form a weld; and thermosonic bonding - using a combination of pressure, elevated temperature, and ultrasonic vibration bursts. The die may be oriented either face up or face down (with its active surface and bond pads either up or down with respect to the circuit board) for wire bonding, although face up orientation is more common. With TAB, ends of metal leads carried on an insulating tape such as a polyimide are respectively attached to the bond pads on the semiconductor die and to the lead or trace ends on the printed circuit board. An encapsulant is generally used to cover the bond wires and metal tape leads to prevent contamination.

Please amend the first full paragraph on page 5 as follows:

One method of increasing integrated circuit density is to stack die vertically. U.S. Patent 5,012,323 ("the '323 patent") issued April 30, 1991 to Farnworth teaches combining a pair of die mounted on opposing sides of a lead frame. An upper, smaller die is back-bonded to the upper surface of the leads of the lead frame via a first adhesively coated, insulated film layer. A lower, larger die is face-bonded to the lower lead frame die-bonding region via a second, adhesively coated, insulative film layer. The wire-bonding pads on both upper die and lower die are interconnected with the ends of their associated lead extensions with gold or aluminum bond wires. The lower die must be slightly larger than the upper die in order ~~that~~ for the die pads ~~are~~ to be accessible from above through a bonding window in the lead frame such that gold wire connections can be made to the lead extensions. This arrangement has a major disadvantage from a production standpoint, since the different size dice require that different equipment produce the different die or that the same equipment be switched over in different production runs to produce the different die.

Please amend the second full paragraph on page 5 as follows:

U.S. Patent 5,291,061 issued March 1, 1994 to Ball teaches a multiple stacked die device containing up to four stacked dice supported on a die-attach paddle of a lead frame, the assembly not exceeding the height of current single die packages, and wherein the bond pads of each die are ~~wirebonded~~ wire bonded to lead fingers. The low profile of the device is achieved by close-tolerance stacking which is made possible by a ~~low-loop-profile wirebonding~~ low-loop-profile wire bonding operation and thin adhesive layers between the stacked dice.

Please amend the third full paragraph on page 5 as follows:

U.S. Patent 5,323,060 issued June 21, 1994 to Fogal et al. teaches a multichip module that contains stacked die devices, the terminals or bond pads of which are ~~wirebonded~~ wire bonded to a substrate or to adjacent die devices.

Please amend the paragraph bridging pages 5 and 6 as follows:

U.S. Patent 5,399,898 issued May 21, 1995 to Rostoker ("Rostoker") teaches multichip, multitier semiconductor arrangements based on single and double-sided ~~flip-chips.~~ flip chips. Rostoker discloses bridging a die over and between two adjacent dice. However, Rostoker intuitively requires the die and bond pad bump patterns be specifically designed to achieve proper electrical communication between the bridged die.

Please amend the first full paragraph on page 6 as follows:

Therefore, it would be advantageous to develop a technique and assembly for increasing integrated circuit density using non-customized die configurations in combination with ~~commercially-available, widely-practiced~~ commercially available, widely practiced semiconductor device fabrication techniques.

Please amend the second full paragraph on page 6 as follows:

The present invention relates to an apparatus and a method for increasing integrated circuit density. The apparatus comprises at least an upper die and an opposing lower die which is connected to a substrate (the term "substrate" will be used for purposes of this application to mean either substrate carrying traces or other conductors, or a leadframe). The lower die is preferably a flip chip having, for example, C4 solder bump connections, conductive polymer bumps, pin connections, or surface mount J-lead connections extending substantially perpendicularly from the face surface of the lower die. The substrate is configured with a specific lead end or trace end pattern compatible with the specific pin out or bump connections on the ~~flip-chip.~~ flip chip.

Please amend the paragraph bridging pages 6 and 7 as follows:

It is, of course, understood that the electrical connection between the upper die and the substrate can be ~~achieve~~ achieved with TAB technology, wherein metal tape leads are attached

between the bond pads on the upper die and the leads on the substrate. However, such an approach obviously requires undesirable pre-planning of bond pad and trace end locations for fabrication of the TAB tape.

Please amend the second full paragraph on page 7 as follows:

Such an arrangement increases semiconductor device density using non-customized die and bond pad patterns, and ~~commercially-practiced~~ commercially practiced conductor attachment techniques.

Please amend the second full paragraph on page 9 as follows:

Preferably, a sealing (underfill) compound 42 as known in the art is disposed between the lower die 14 and the substrate 16 to prevent contamination of the ~~die-to-substrate~~ die-to-substrate board connections 20 and to more firmly secure the lower die 14 to the substrate 16. A glob top 48 may be applied over assembly 10 individually as shown in broken lines, or over the entire substrate 16, which may support a plurality of assemblies 10. The ~~subsequently-described~~ subsequently described embodiments may similarly be ~~glob-topped,~~ glob-topped, as desired.

Please amend the first full paragraph on page 10 as follows:

A back side 52 of a second die 54 is adhered to the lower die 14 with the layer of adhesive 28 applied over the lower die back side 30. A face side 56 of the second die 54 has a plurality of bond pads 58 disposed thereon. A plurality of bond wires 60 is attached between the second die bond pads 58 and corresponding trace or lead ends 40 on the upper surface 24 of the substrate 16. Additionally, as shown in FIG. 2, if the second die 54 is slightly smaller than the lower die 14, an additional component 62, such as a resistor, capacitor, or the like, may be adhered to the layer of adhesive 28 on the lower die back side 30. This arrangement frees up space on the substrate 16 that would normally be taken up by the component 62. A second ~~die-to-component~~ die-to-component bond wire 64 is attached between a respective second die

bond pad 58 and the component 62. A component-to-substrate bond wire 66 is attached between the component 62 and trace or lead end 40 on the upper surface 24 of the substrate 16.

Please amend the second full paragraph on page 10 as follows:

A back side 68 of a third die 70 is adhered to the second die 54 with a second layer of adhesive 72 applied on the second die face side 56. A face side 74 of the third die 70 has a plurality of bond pads 76 disposed thereon. A plurality of bond wires 78 is attached between the third die bond pads 76 and corresponding trace or lead ends 40 on the upper surface 24 of the substrate 16. Wire bonds could also be made from third die 70 to component 62, or to yet another discrete component stacked on and adhered to third die 70.

Please amend the third full paragraph on page 10 as follows:

FIG. 3 illustrates another alternative bare die assembly 80, comprising a second discrete component 82 adhered to the second layer of adhesive 72. A third die-to-component bond wire 84 is attached between a respective third die bond pad 76 and the component 62. A first component-to-substrate bond wire 66 is attached between the component 62 and the upper surface 24 of the substrate 16. A third~~-die-to-second-~~ die-to-second component bond wire 86 is attached between a respective second die bond pad 76 and the second component 82. A second component-to-substrate bond wire 88 is attached between the component 82 and the upper surface 24 of the substrate 16.

Please amend the third full paragraph on page 11 as follows:

The back side 68 of the third die 70 is adhered to the second die 54 with the second layer of adhesive 72 applied on the second die face side 56. The face side 74 of the third die 70 has a plurality of bond pads 76 disposed thereon. A plurality of bond wires 78 is attached between the third die bond pads 76 and corresponding trace or lead ends 40 on the upper surface 24 of the substrate 16. A third~~-die-to-component-~~ die-to-component bond wire 96 is attached between a

respective third die bond pad 76 and the component 62A. A second component-to-substrate bond wire 98 is attached between the component 62A to the upper surface 24 of the substrate 16.

Please amend the second full paragraph on page 12 as follows:

The back side 52 of second die 54 bridges and is adhered to both lower dice 14A and 14B with the layers of adhesive 28A and 28B applied over the lower die back sides 30A and 30B. The face side 56 of the second die 54 has a plurality of bond pads 58 disposed thereon. A plurality of bond wires 60 is attached between the second die bond pads 58 and corresponding trace or lead ends 40 on the upper surface 24 of the substrate 16. An additional component 62, such as a resistor, capacitor, or the like, may be adhered to substrate or leadframe 16 by a layer of ~~adhesive 64.~~ adhesive 65. A second die-to-component bond wire 92 is attached between a respective first die bond pad 58 and the component 62. A component-to-substrate bond wire 94 is attached between the component 62 and the upper surface 24 of the substrate 16.